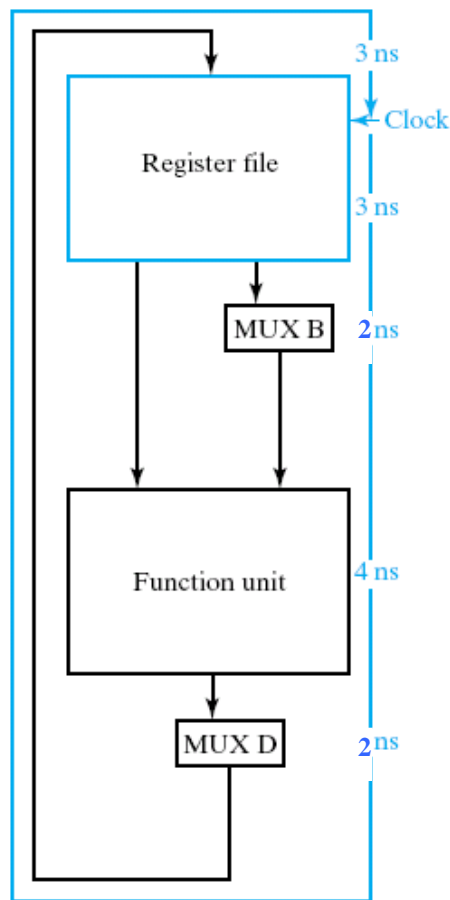


Tutorial 9

RISC and CISC

CO 2206 Computer Organization

Task 1. Single-Cycle Computer Clock Limit



Processing of a microoperation involves fetching the operand(s) from the register file and appropriately select the multiplex MUX B, selecting and performing the requested operation on the operand(s), appropriately selecting the result/data at the multiplexer MUX D and finally writing the result/data back to the register. These events process the microoperation through the datapath. Figure to the left shows the datapath of an example CPU. If the times required to pass through the different circuitry in the datapath is as shown in the figure, determine the maximum clock frequency that can be used with this CPU.

Task 2. Pipelining

- What is the purpose of using pipelining?
- Define latency and instruction throughput?
- Will pipelining decrease or increase latency time?
- Will pipelining decrease or increase instruction throughput?
- Determine the latency and instruction throughput when executing 3 instructions in a computer using 4-stage pipelining and a clock speed of 500MHz.

Task 3. Hazards in Pipelining

- What is data hazard in a pipelined datapath? Illustrate your explanation using appropriate example.
- Using appropriate illustrations, explain how data forwarding overcome data hazards.

Task 4. RISC

- Referring to the RISC computer described in the lecture, answer the following questions:
 - What does it mean by hardwired control unit? What would be used if it the control unit was not hardwired?
 - Why does the processor require increased amount of registers, as compared to the single-cycle computer described in Chapter 8?
 - What is the maximum number of distinct instructions that can be specified? Explain how this number is derived.
 - How many bits does the immediate (constant) field has? Why do we need to perform zero fill or sign extend on the constant?
 - Referring to the instruction set given in the lecture slide, give one example for each of the four addressing modes below:
 - Register
 - Register Indirect
 - Immediate
 - Relative