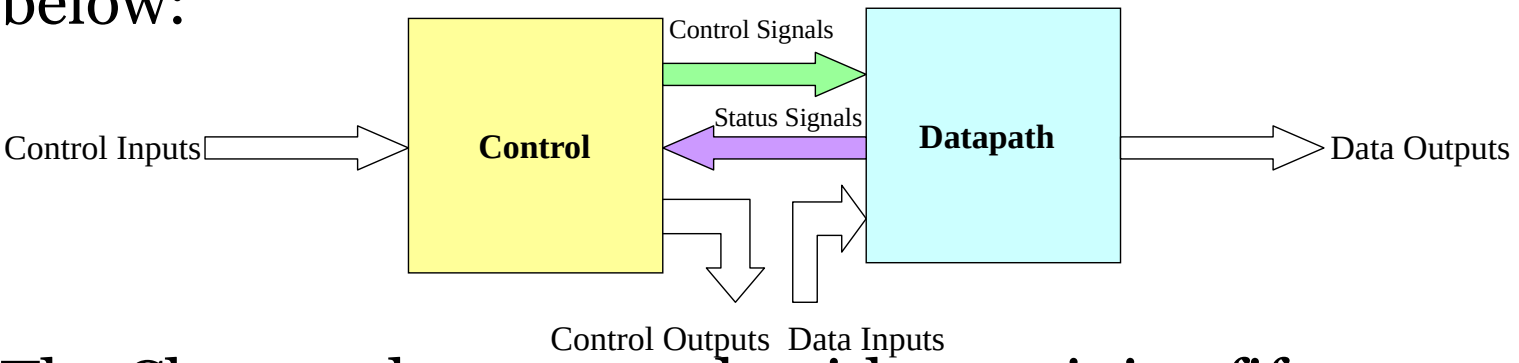
Tutorial 8
Computer Design Basics

CO 2206 Computer Organization

Task 1.1

- The first slide of Chapter 8 starts with a block diagram below:



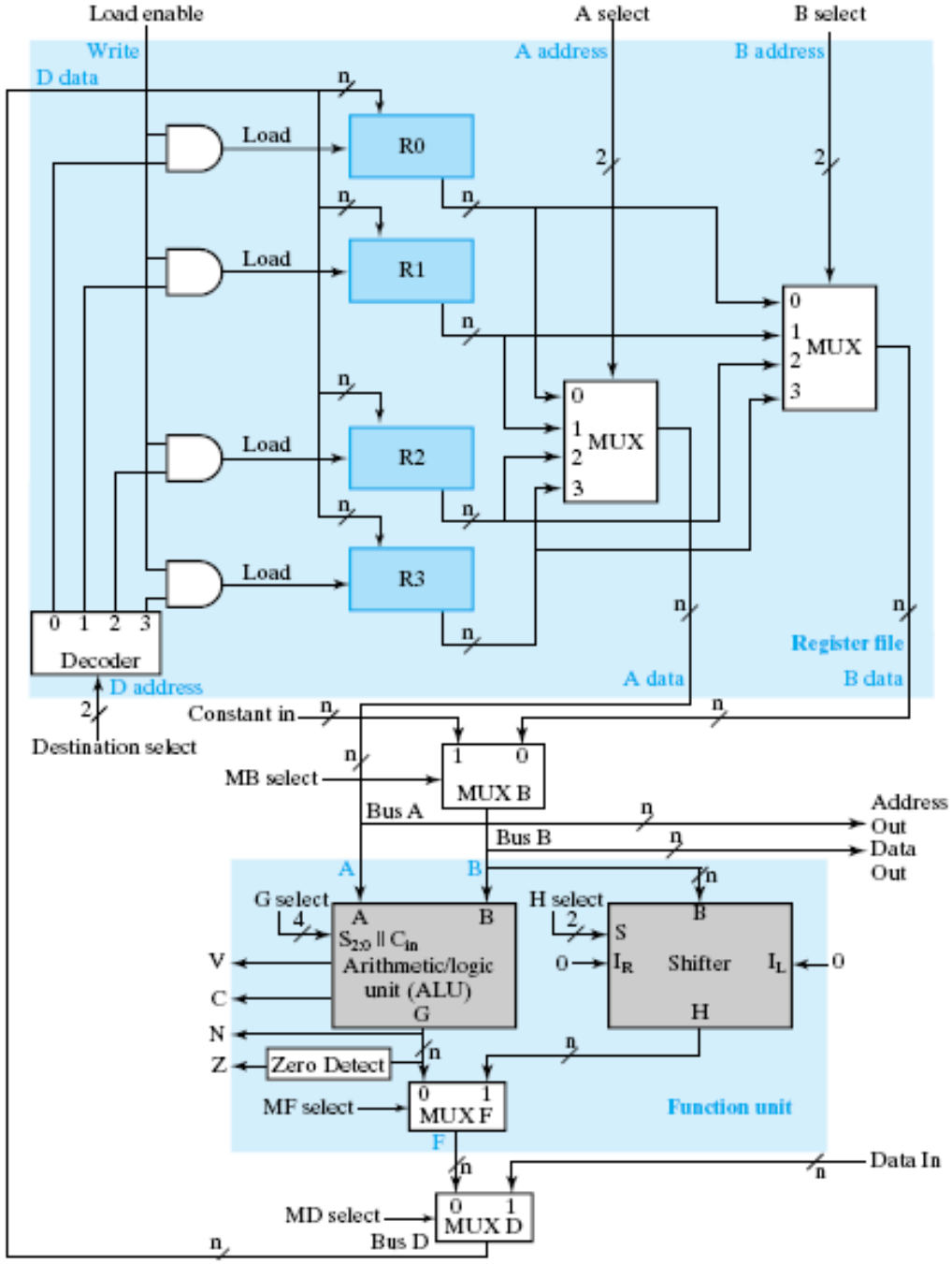
- The Chapter then proceeds with remaining fifty over slides to explain some computer design basics. In your own words, explain the above block diagram making use of the following terms:
- *CPU, ALU, Registers, Selection Logic, Instruction Decoder, Instruction, Control Word, Operation, Microoperation, Control Bus, Address Bus, Data Bus*

Task 1.2

- Answer the following questions, with reference to the block diagram (and your explanation) in previous slide:
  - What make up the Control Inputs and where do they come from?
  - What make up the Control Signals?
  - What make up the Status Signals?
  - What make up the Data Outputs and where do they go to?

Task 2.1

- This simple Datapath block diagram is the same circuitry that has been studied in the lectures. The ALU in the Datapath has the following (next slide) function table.



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Task 2.2

Function Table for ALU

Operation Select					
S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	$G \leftarrow A$	Transfer A
0	0	0	1	$G \leftarrow A + 1$	Increment A
0	0	1	0	$G \leftarrow A + B$	Addition
0	0	1	1	$G \leftarrow A + B + 1$	Add with carry input of 1
0	1	0	0	$G \leftarrow A + \overline{B}$	A plus 1's complement of B
0	1	0	1	$G \leftarrow A + \overline{B} + 1$	Subtraction
0	1	1	0	$G \leftarrow A + 1$	Decrement A
0	1	1	1	$G \leftarrow A$	Transfer A
1	X	0	0	$G \leftarrow A \wedge B$	AND
1	X	0	1	$G \leftarrow A \vee B$	OR
1	X	1	0	$G \leftarrow A \oplus B$	XOR
1	X	1	1	$G \leftarrow \overline{A}$	NOT (1's complement)

Task 2.3

- Answer the following questions, with reference to the above (previous slides) information:
  - State the three major steps to perform an ALU microoperation.
  - The G select is used to specify the required ALU microoperation, what is the maximum number of distinct ALU microoperations that can be specified?
  - Explain clearly the steps (including values of all necessary select signals), in sequence, to perform the microoperation of R1 ← R2 AND R3.

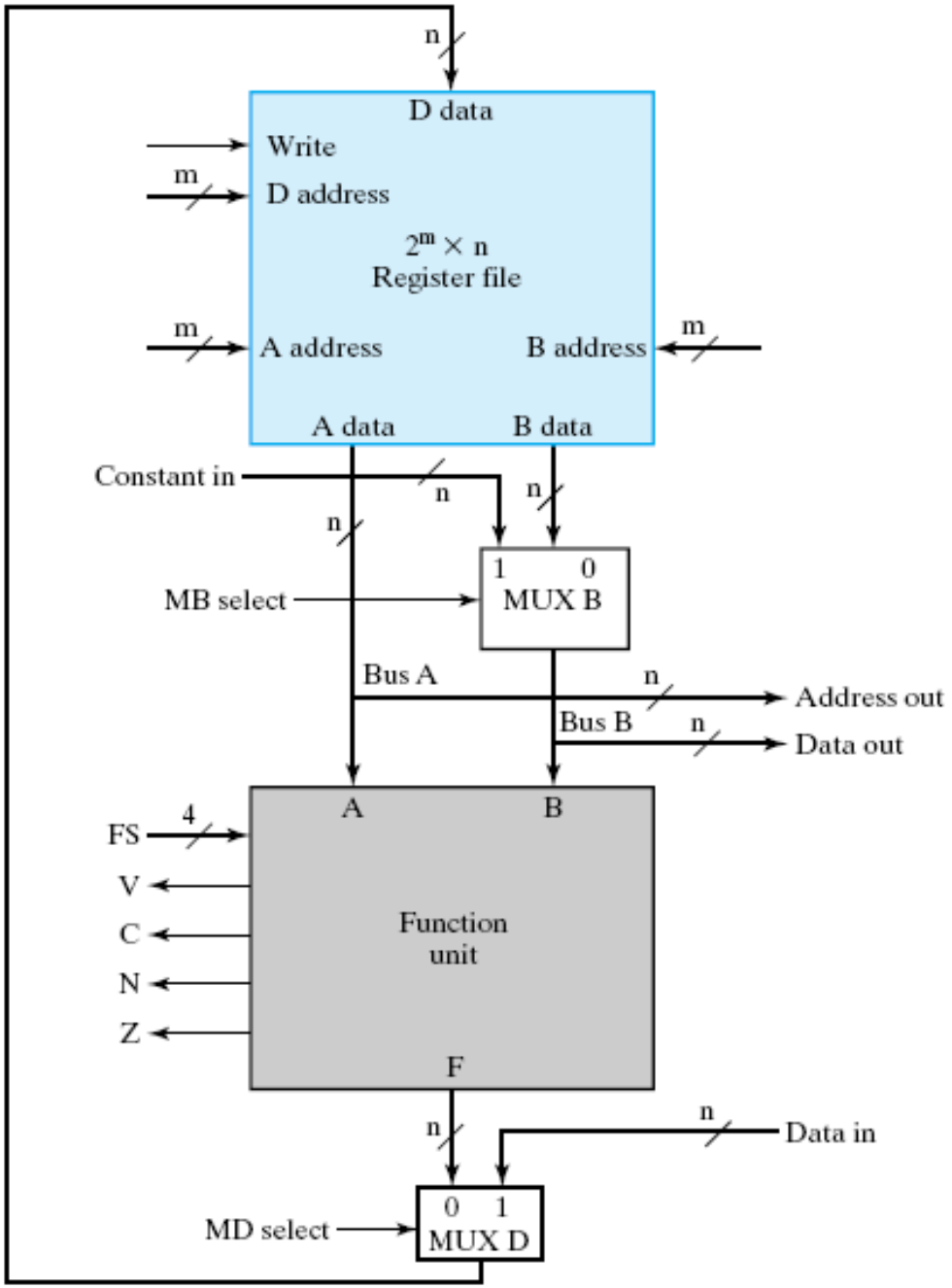
Task 3

- You are required to design an 8-bit barrel shifter as follow:
  - Draw the logic diagram using 3x8 multiplexers only.
  - Draw the function table, specifying the operation for each combination of select signals.
  - State the maximum number of position that the shifter can shift to left.
  - State the maximum number of position that the shifter can shift to right.

Task 4.1

- The following (next slide) block diagram of a Datapath can be used as a higher level representation of the Datapath in Task 2. Referring to the block diagrams in this task and Task 2, answer the following questions:
  - What is the value of m?
  - What does the Register File consist of?
  - What does the Function Unit consist of?
  - What is missing in the block diagram of Task 2, within the Function Unit? Hint: See Task 5.

Task 4.2



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Task 5.1

- Table below (next slide) shows the relation defined between function select FS and the internal selects G (G3G2G1G0), H (H1H0) and MF within the function unit. Using K-Map, determine the Boolean functions required to implement the following internal signals from FS (F3F2F1F0):
  - MF
  - H1 and H0
  - G3, G2, G1 and G0

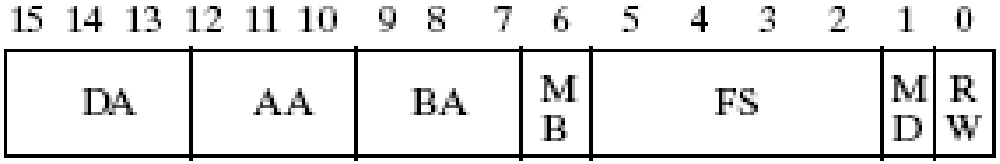
Task 5.2

***G* Select, *H* Select, and *MF* Select Codes Defined in Terms of *FS* Codes**

FS(3:0)	MF Select	G Select(3:0)	H Select	Microoperation
0000	0	0000	XX	$F \leftarrow A$
0001	0	0001	XX	$F \leftarrow A + 1$
0010	0	0010	XX	$F \leftarrow A + B$
0011	0	0011	XX	$F \leftarrow A + B + 1$
0100	0	0100	XX	$F \leftarrow A + \overline{B}$
0101	0	0101	XX	$F \leftarrow A + \overline{B} + 1$
0110	0	0110	XX	$F \leftarrow A - 1$
0111	0	0111	XX	$F \leftarrow A$
1000	0	1X00	XX	$F \leftarrow A \wedge B$
1001	0	1X01	XX	$F \leftarrow A \vee B$
1010	0	1X10	XX	$F \leftarrow A \oplus B$
1011	0	1X11	XX	$F \leftarrow \overline{A}$
1100	1	XXXX	00	$F \leftarrow B$
1101	1	XXXX	01	$F \leftarrow \text{sr } B$
1110	1	XXXX	10	$F \leftarrow \text{sl } B$

Task 6.1

- For the same Datapath architecture shown in Task 4, with m=3, the following Control Word format is adopted:



- Assuming the following (next slide) encoding is used, determine the Control Word required to perform the following microoperation:
  - R1 ← R2 AND R5
  - R0 ← R0 + 3
  - R4 ← shift right R6
  - R7 ← 5
  - Data Out ← R0

Task 6.2

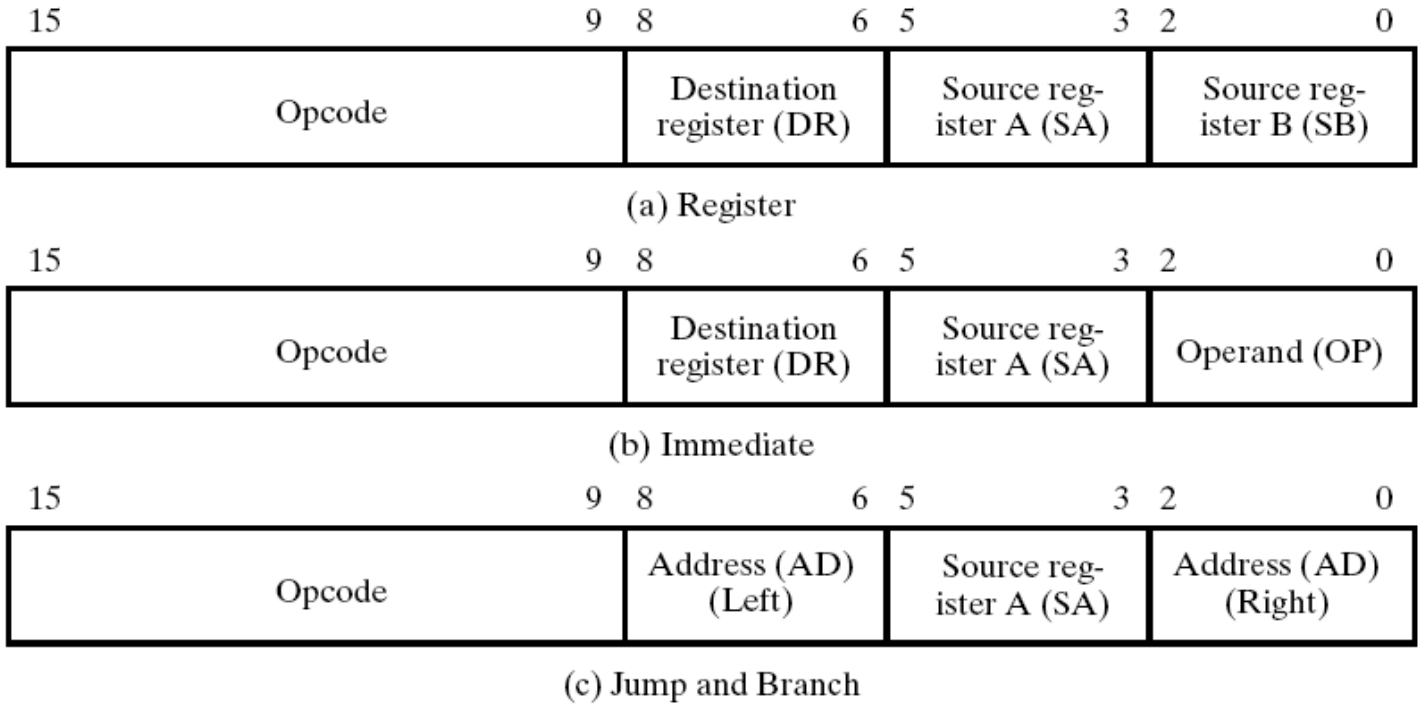
Encoding of Control Word for the Datapath

DA, AA, BA		MB		FS		MD		RW	
Function	Code	Function	Code	Function	Code	Function	Code	Function	Code
$R0$	000	Register	0	$F \leftarrow A$	0000	Function	0	No write	0
$R1$	001	Constant	1	$F \leftarrow A + 1$	0001	Data In	1	Write	1
$R2$	010			$F \leftarrow A + B$	0010				
$R3$	011			$F \leftarrow A + B + 1$	0011				
$R4$	100			$F \leftarrow A + \overline{B}$	0100				
$R5$	101			$F \leftarrow A + \overline{B} + 1$	0101				
$R6$	110			$F \leftarrow A - 1$	0110				
$R7$	111			$F \leftarrow A$	0111				
				$F \leftarrow A \wedge B$	1000				
				$F \leftarrow A \vee B$	1001				
				$F \leftarrow A \oplus B$	1010				
				$F \leftarrow \overline{A}$	1011				
				$F \leftarrow B$	1100				
				$F \leftarrow \text{sr } B$	1101				
				$F \leftarrow \text{sl } B$	1110				

Task 7.1

- If the below (next slide) instruction format is adopted and by referring to the instruction set given in the lecture slide, determine the necessary instructions (in machine code) to specify the five microoperations in Task 6. In addition, answer the following questions:
  - How many distinct instructions can be specified by the Opcode?
  - What is the maximum unsigned immediate operand that can be provided?
  - What is the highest branch range?

Task 7.2


15
9
8
6
5
3
2
0
Opcode
Destination register (DR)
Source register A (SA)
Source register B (SB)
(a) Register
15
9
8
6
5
3
2
0
Opcode
Destination register (DR)
Source register A (SA)
Operand (OP)
(b) Immediate
15
9
8
6
5
3
2
0
Opcode
Address (AD) (Left)
Source register A (SA)
Address (AD) (Right)
(c) Jump and Branch

Task 8

- Briefly state the two issues of single-cycle computer highlighted in lecture slides.