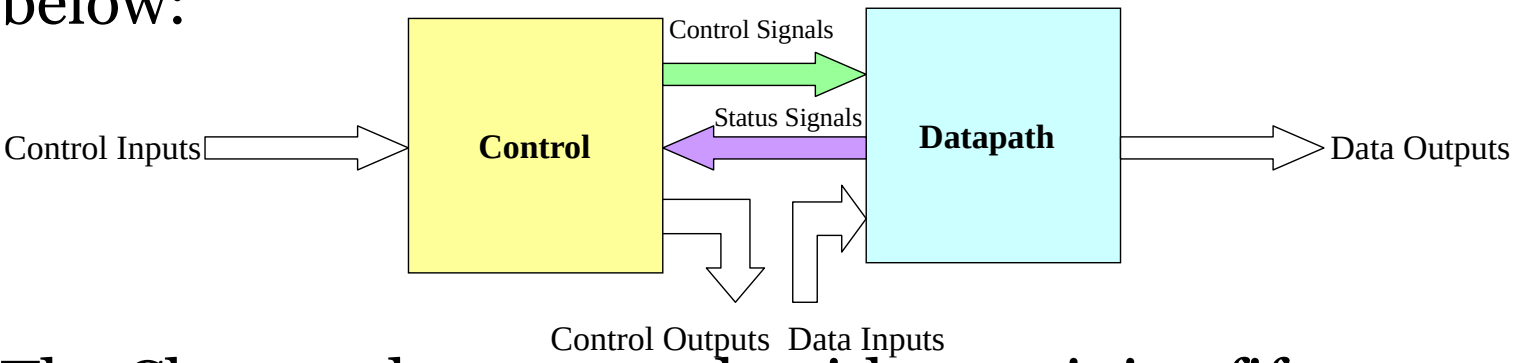
Tutorial 8 – Sample Solutions
Computer Design Basics

CO 2206 Computer Organization

Task 1.1

- The first slide of Chapter 8 starts with a block diagram below:



- The Chapter then proceeds with remaining fifty over slides to explain some computer design basics. In your own words, explain the above block diagram making use of the following terms:
- *CPU, ALU, Registers, Selection Logic, Instruction Decoder, Instruction, Control Word, Operation, Microoperation, Control Bus, Address Bus, Data Bus*

Task 1.2

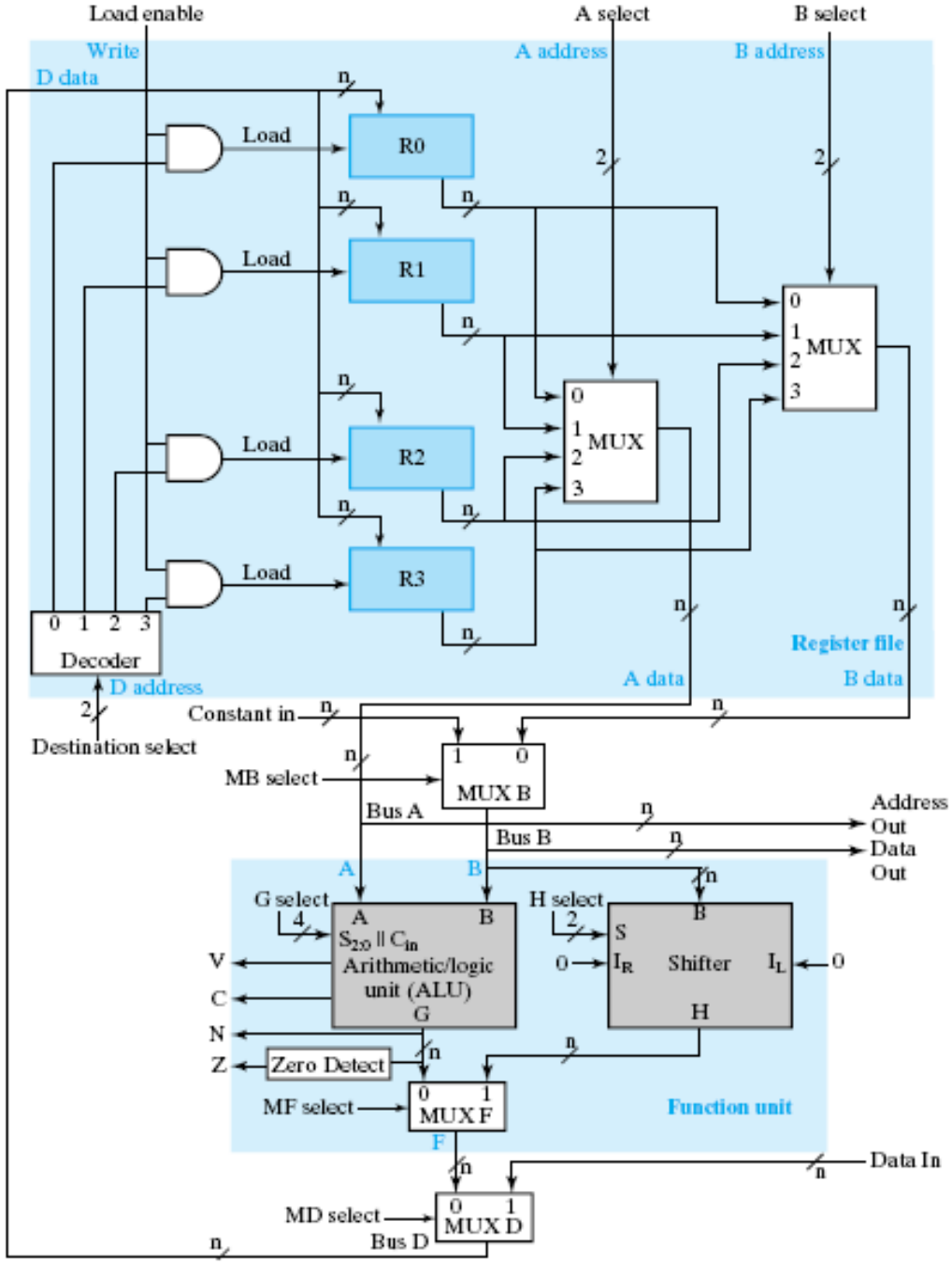
- Answer the following questions, with reference to the block diagram (and your explanation) in previous slide:
  - What make up the Control Inputs and where do they come from?
  - What make up the Control Signals?
  - What make up the Status Signals?
  - What make up the Data Outputs and where do they go to?

Task 1. Ans

- Description – refer lecture slides and reference material.
  - Program instructions are the inputs to the control section of the CPU. These instructions are fetched from the memory (through data bus). The instructions (program) are written by programmer (human). In short, human control the CPU.
  - The Control Word provides the Control Signals to the datapath.
  - The Status Signals are signals from the ALU providing information regarding the result of current ALU operation, such as overflow, zero, negative.
  - Data Outputs are data from specific register being placed on the data bus. These outputs are being transferred to memory or other external devices.

Task 2.1

- This simple Datapath block diagram is the same circuitry that has been studied in the lectures. The ALU in the Datapath has the following (next slide) function table.



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Task 2.2

Function Table for ALU

Operation Select					
S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	$G \leftarrow A$	Transfer A
0	0	0	1	$G \leftarrow A + 1$	Increment A
0	0	1	0	$G \leftarrow A + B$	Addition
0	0	1	1	$G \leftarrow A + B + 1$	Add with carry input of 1
0	1	0	0	$G \leftarrow A + \overline{B}$	A plus 1's complement of B
0	1	0	1	$G \leftarrow A + \overline{B} + 1$	Subtraction
0	1	1	0	$G \leftarrow A + 1$	Decrement A
0	1	1	1	$G \leftarrow A$	Transfer A
1	X	0	0	$G \leftarrow A \wedge B$	AND
1	X	0	1	$G \leftarrow A \vee B$	OR
1	X	1	0	$G \leftarrow A \oplus B$	XOR
1	X	1	1	$G \leftarrow \overline{A}$	NOT (1's complement)

Task 2.3

- Answer the following questions, with reference to the above (previous slides) information:
  - State the three major steps to perform an ALU microoperation.
  - The G select is used to specify the required ALU microoperation, what is the maximum number of distinct ALU microoperations that can be specified?
  - Explain clearly the steps (including values of all necessary select signals), in sequence, to perform the microoperation of R1 ← R2 AND R3.

Task 2. Ans (1)

- 3 major steps to perform an ALU microoperation (note: NOT perform instruction):
  - The contents of specified source registers are applied to the inputs of the ALU
  - ALU performs an operation
  - Result transferred to a destination register
- G select has 4 lines giving 24 =16 possible distinct operations to be specified (0000b to 1111b)

Task 2. Ans (2)

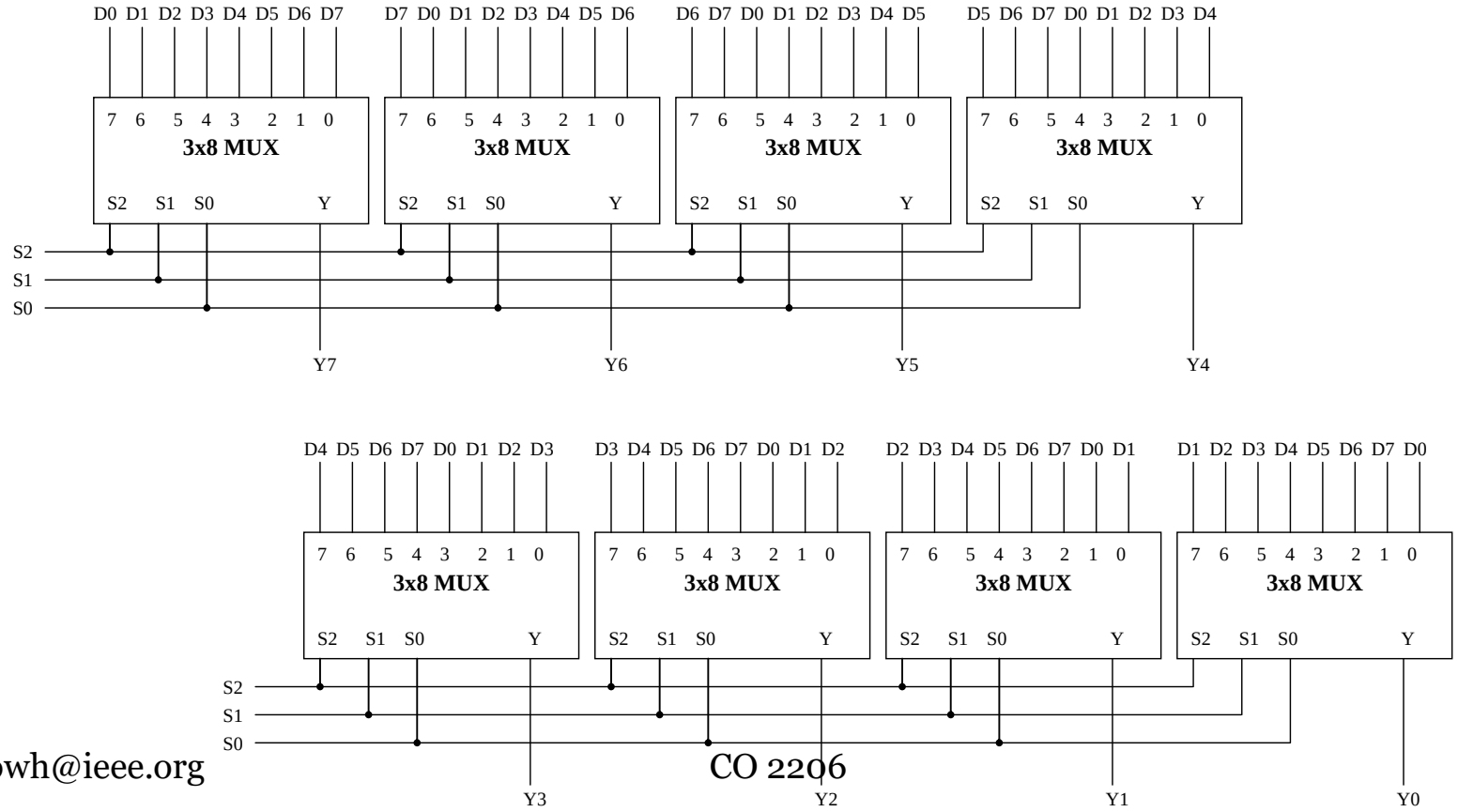
- Steps in performing microoperation: R1 ← R2 AND R3
  - Apply 10 to A select to place content of R2 onto Bus A
  - Apply 11 to B select to place content of R3 onto B data and apply 0 to MB select to place B data on Bus B
  - Apply 1000 (1x00, making x=0) to G select to perform anding G = Bus A AND Bus B
  - Apply 0 to MF select and 0 to MD select to place the value of G onto BUS D
  - Apply 01 to Destination select to enable the Load input to R1
  - Apply 1 to Load Enable to force the Load input to R1 to 1 so that R1 is loaded on next clock pulse
  - The overall microoperation requires 1 clock cycle

Task 3

- You are required to design an 8-bit barrel shifter as follow:
  - Draw the logic diagram using 3x8 multiplexers only.
  - Draw the function table, specifying the operation for each combination of select signals.
  - State the maximum number of position that the shifter can shift to left.
  - State the maximum number of position that the shifter can shift to right.

Task 3. Ans (1)

- 8-bit requires 8 multiplexers (3x8 MUX). Note that a 3x8 MUX has 3 selection lines to select one of the 8 inputs to be connected to the output. Logic diagram:



Task 3. Ans (2)

- Function table:

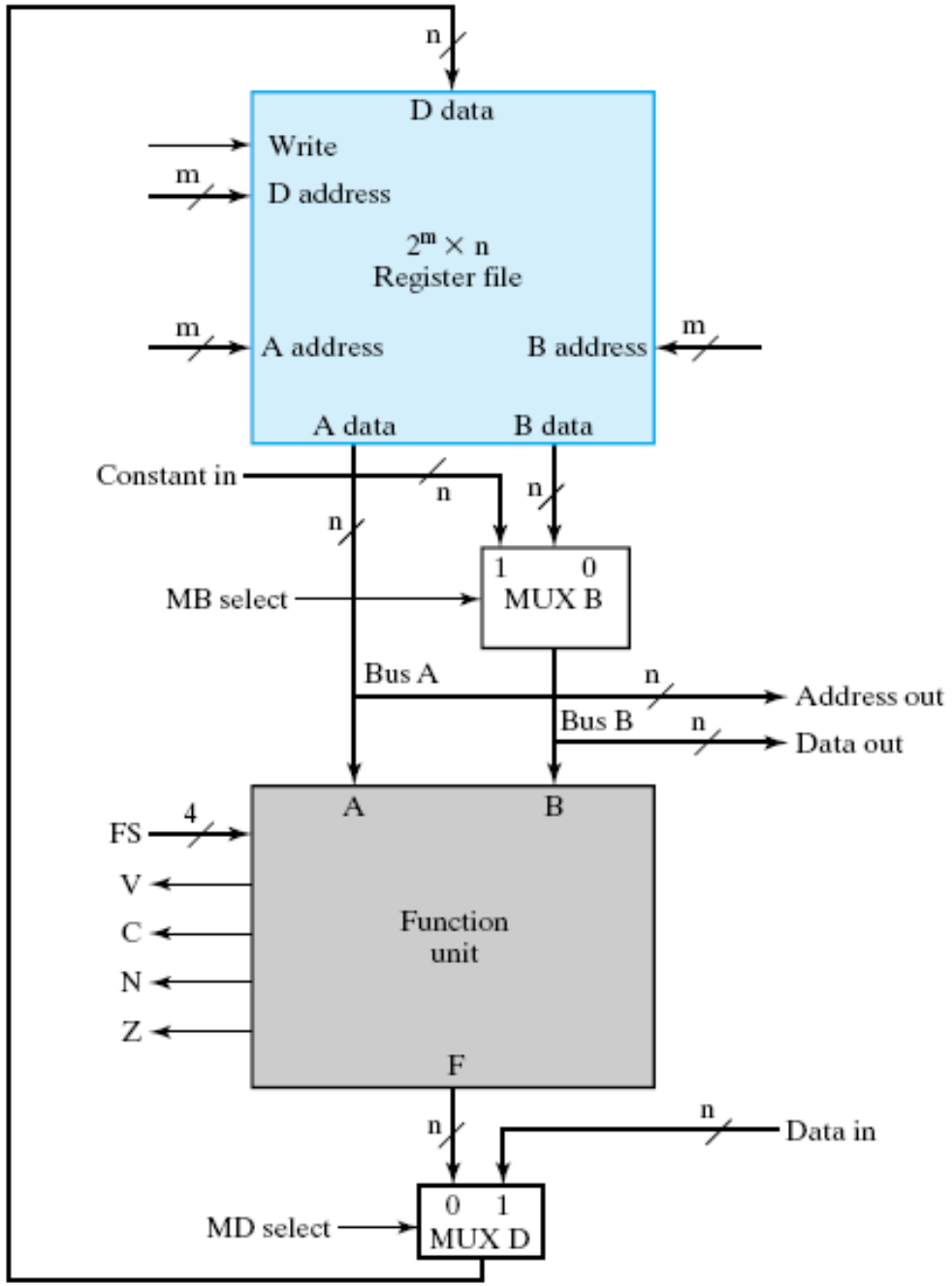
Select			Output								Operation
S2	**S1**	**S0**	**Y7**	**Y6**	**Y5**	**Y4**	**Y3**	**Y2**	**Y1**	**Y0**	
0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	No rotation
0	0	1	D6	D5	D4	D3	D2	D1	D0	D7	Rotate 1 position to left
0	1	0	D5	D4	D3	D2	D1	D0	D7	D6	Rotate 2 position to left
0	1	1	D4	D3	D2	D1	D0	D7	D6	D5	Rotate 3 position to left
1	0	0	D3	D2	D1	D0	D7	D6	D5	D4	Rotate 4 position to left
1	0	1	D2	D1	D0	D7	D6	D5	D4	D3	Rotate 5 position to left
1	1	0	D1	D0	D7	D6	D5	D4	D3	D2	Rotate 6 position to left
1	1	1	D0	D7	D6	D5	D4	D3	D2	D1	Rotate 7 position to left

- 7 left (when Select =111)
- 7 right (when Select =001)

Task 4.1

- The following (next slide) block diagram of a Datapath can be used as a higher level representation of the Datapath in Task 2. Referring to the block diagrams in this task and Task 2, answer the following questions:
  - What is the value of m?
  - What does the Register File consist of?
  - What does the Function Unit consist of?
  - What is missing in the block diagram of Task 2, within the Function Unit? Hint: See Task 5.

Task 4.2



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Task 4. Ans

- M =2 as seen from the Destination Select in the block diagram in Q2
- Register file in Q4 consists of the 4 registers, 4 AND gates, 1 2x4 decoder and 2 2x4 multipliers in Q2
- Function unit in Q4 consists of the ALU, Shifter, multiplixer MUX F and zero detect circuit in Q2
- The block diagram in Q2 has G (4-bit) and H (2-bit) selects, while the block diagram in Q4 has FS (4-bit) select. There should be a logic circuit in the Function unit of Q4 to convert the value of FS into correct values of G and H.

Task 5.1

- Table below (next slide) shows the relation defined between function select FS and the internal selects G (G3G2G1G0), H (H1H0) and MF within the function unit. Using K-Map, determine the Boolean functions required to implement the following internal signals from FS (F3F2F1F0):
  - MF
  - H1 and H0
  - G3, G2, G1 and G0

Task 5.2

***G* Select, *H* Select, and *MF* Select Codes Defined in Terms of *FS* Codes**

FS(3:0)	MF Select	G Select(3:0)	H Select	Microoperation
0000	0	0000	XX	$F \leftarrow A$
0001	0	0001	XX	$F \leftarrow A + 1$
0010	0	0010	XX	$F \leftarrow A + B$
0011	0	0011	XX	$F \leftarrow A + B + 1$
0100	0	0100	XX	$F \leftarrow A + \overline{B}$
0101	0	0101	XX	$F \leftarrow A + \overline{B} + 1$
0110	0	0110	XX	$F \leftarrow A - 1$
0111	0	0111	XX	$F \leftarrow A$
1000	0	1X00	XX	$F \leftarrow A \wedge B$
1001	0	1X01	XX	$F \leftarrow A \vee B$
1010	0	1X10	XX	$F \leftarrow A \oplus B$
1011	0	1X11	XX	$F \leftarrow \overline{A}$
1100	1	XXXX	00	$F \leftarrow B$
1101	1	XXXX	01	$F \leftarrow \text{sr } B$
1110	1	XXXX	10	$F \leftarrow \text{sl } B$

Task 5. Ans (1)

- The above table shows 4-bit input FS (F3||F0) and 7-bit output MF, G (G3||G0) and H (H1||H0). To determine the logic function to necessary to convert FS into correct values of MF, G and H, we treat each output bit (each output column) individually (one K-map each). Note that FS =1111 is not used and can be treated as don't care for all outputs.

Task 5. Ans (2)

$MF = F_3F_2$

F_2 \ F_1	0	0	0	0
0	0	0	0	0
1	1	1	x	1
0	0	0	0	0

F_3 | F_0

$H_1 = F_1$

F_2 \ F_1	x	x	x	x
x	x	x	x	x
0	0	x	1	x
x	x	x	x	x

F_3 | F_0

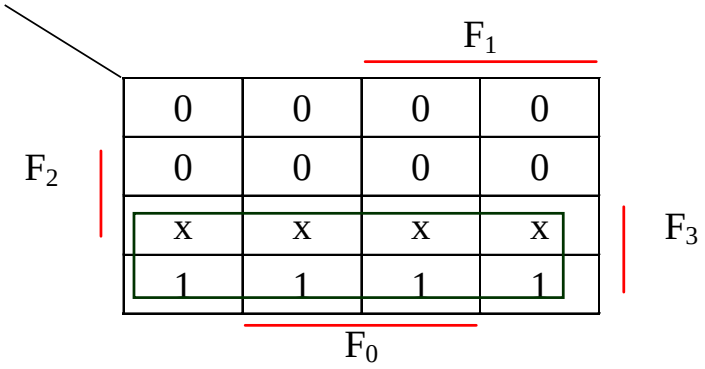
$H_0 = F_0$

F_2 \ F_1	x	x	x	x
x	x	x	x	x
0	1	x	0	x
x	x	x	x	x

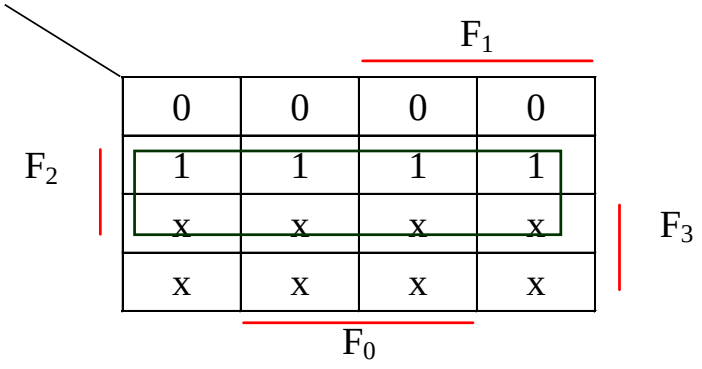
F_3 | F_0

Task 5. Ans (3)

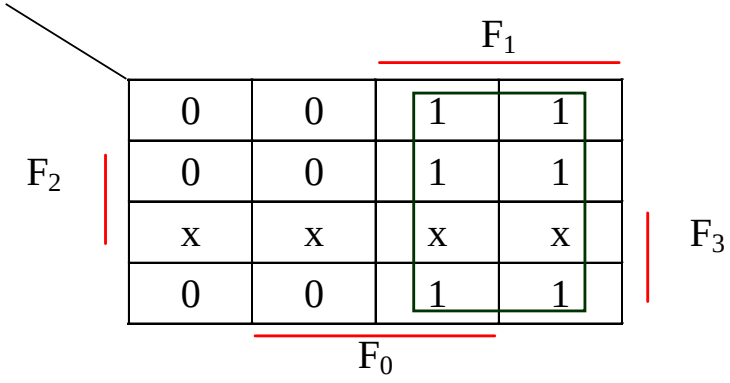
$G_3 = F_3$



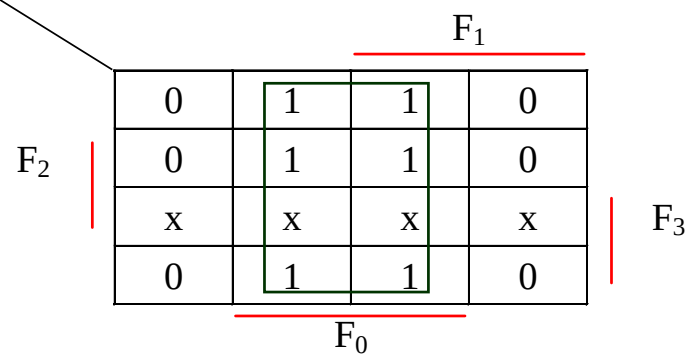
$G_2 = F_2$



$G_1 = F_1$

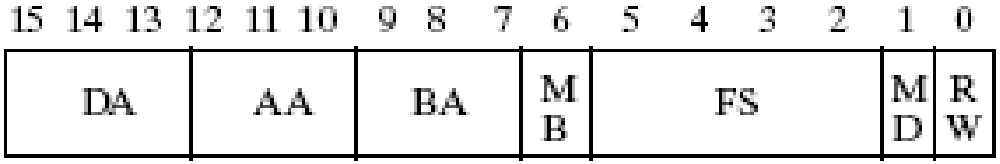


$G_0 = F_0$



Task 6.1

- For the same Datapath architecture shown in Task 4, with m=3, the following Control Word format is adopted:



- Assuming the following (next slide) encoding is used, determine the Control Word required to perform the following microoperation:
  - R1 ← R2 AND R5
  - R0 ← R0 + 3
  - R4 ← shift right R6
  - R7 ← 5
  - Data Out ← R0

Task 6.2

Encoding of Control Word for the Datapath

DA, AA, BA		MB		FS		MD		RW	
Function	Code	Function	Code	Function	Code	Function	Code	Function	Code
$R0$	000	Register	0	$F \leftarrow A$	0000	Function	0	No write	0
$R1$	001	Constant	1	$F \leftarrow A + 1$	0001	Data In	1	Write	1
$R2$	010			$F \leftarrow A + B$	0010				
$R3$	011			$F \leftarrow A + B + 1$	0011				
$R4$	100			$F \leftarrow A + \overline{B}$	0100				
$R5$	101			$F \leftarrow A + \overline{B} + 1$	0101				
$R6$	110			$F \leftarrow A - 1$	0110				
$R7$	111			$F \leftarrow A$	0111				
				$F \leftarrow A \wedge B$	1000				
				$F \leftarrow A \vee B$	1001				
				$F \leftarrow A \oplus B$	1010				
				$F \leftarrow \overline{A}$	1011				
				$F \leftarrow B$	1100				
				$F \leftarrow \text{sr } B$	1101				
				$F \leftarrow \text{sl } B$	1110				

Task 6. Ans (1)

- Destination DA =R1 =001, Source1 AA =R2 =010, Source2 BA =R5 =101, MB =Source2 is register =0, Operation FS =(F ← A ∧ B) =1000, MD =result from Function unit =0, RW =destination register to be Written =1, **Control Word =0010,1010,1010,0001 =2AA1h**
- Destination DA =R0 =000, Source1 AA =R0 =000, Source2 BA =none =000 (any value), MB =Source2 is Constant in =1, Operation FS =(F ← A + B) =0010, MD =result from Function unit =0, RW =destination register to be Written =1, **Control Word =0000,0000,0100,1001 =0049h**
- Destination DA =R4 =100, Source1 AA =none =000 (any value), Source2 BA =R6 =110, MB =Source2 is register =0, Operation FS =(F ← sr B) =1101, MD =result from Function unit =0, RW =destination register to be Written =1, **Control Word =1000,0011,0011,0101 =8335h**

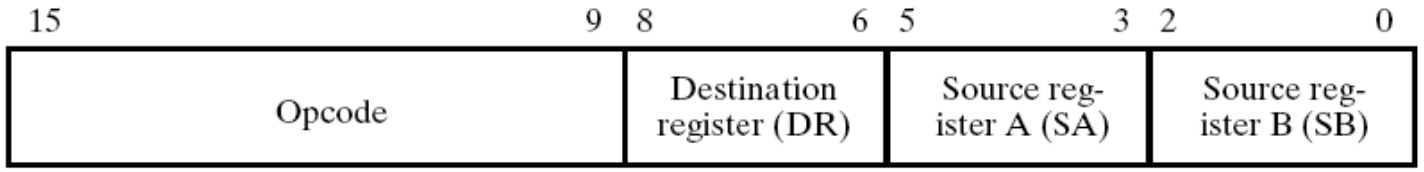
Task 6. Ans (2)

- Destination DA =R7 =111, Source1 AA =none =000 (any value), Source2 BA =none =000 (any value), MB =not important =0 (any value), Operation FS =not important =0000 (any value), MD =result from Data in =1, RW =destination register to be Written =1, **Control Word =1110,0000,0000,0011 =E003h**
- Destination DA =none =000 (any value), Source1 AA =none =000 (any value), Source2 BA =R0 =000 (to go to Bus B and Data out), MB =Source2 is register =0 (B selected to Data out, microoperation done), Operation FS =not important =0000 (any value), MD =not important =0 (any value), RW =destination register NOT to be Written =0, **Control Word =0000,0000,0000,0000 =0000h**
- Note: If R0 is Read Only, (b) is invalid.

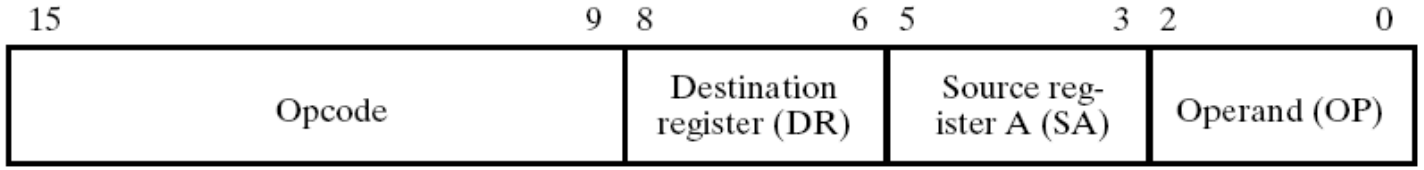
Task 7.1

- If the below (next slide) instruction format is adopted and by referring to the instruction set given in the lecture slide, determine the necessary instructions (in machine code) to specify the five microoperations in Task 6. In addition, answer the following questions:
  - How many distinct instructions can be specified by the Opcode?
  - What is the maximum unsigned immediate operand that can be provided?
  - What is the highest branch range?

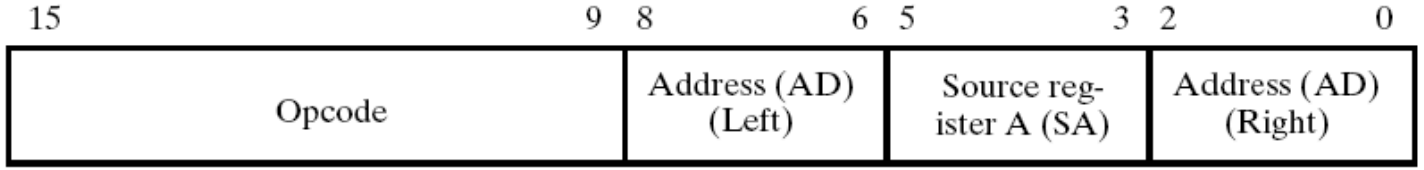
Task 7.2



(a) Register



(b) Immediate



(c) Jump and Branch

Task 7. Ans (1)

- Getting values of DA, AA, BA from pervious answers and referring to instruction set in lecture slide:
- Use Register format. DR =DA =R1 =001, SA =AA =R2 =010, SB =BA =R5 =101, Opcode (from instruction set) =AND =0001000, **Machine Code =0001,0000,0101,0101 =1055h**
- Use Immediate format. DR =DA =R0 =000, SA =AA =R0 =000, OP =3 =011, Opcode (from instruction set) =ADI =1000010, **Machine Code =1000,0100,0000,0011 =1055h**
- Use Register format. DR =DA =R4 =100, SA =none =000 (any value), SB =BA =R6 =110, Opcode (from instruction set) =SHR =0001101, **Machine Code =0001,1011,0000,0110 =1B06h**
- Use Immediate format. DR =DA =R7 =111, SA =none =000 (any value), OP =5 =101, Opcode (from instruction set) =LDI =1001100, **Machine Code =1001,1001,1100,0101 =99C5h**

Task 7. Ans (2)

- Use Register format. Data Out has to be going to external device with an address. The destination address shall be stored in a register. Assuming destination address being stored in R7. DR =none =000 (any value), SA =register holding memory address =R7 =111, SB =BA =R0 =000, Opcode (from instruction set) =ST =0100000, **Machine Code =0100,0000,0011,1000 =4038h**

- Opcode field is 7 bits long giving 27 =128 combinations, hence capable of specifying up to 128 distinct instructions.
- Operand field is 3 bits long. It can specify unsigned operand from 000 to 111. Hence, maximum unsigned immediate operand is 7 (111).
- Branch range is given by AD left (3 bits) concatenated with AD right (3 bits), in 2's complement format. Hence, maximum range is 100,000 (largest negative number) to 011,111 (largest positive number), i.e. –25 to (25 – 1) or –32 to 31.

Task 8

- Briefly state the two issues of single-cycle computer highlighted in lecture slides.

- Ans.
- Requires two distinct memories
- Has a lower limit in clock period based on the worst delay path