# Tutorial 6 - Sample Solution Sequential Circuit 

CO 2206 Computer Organization

## Task 1

- A sequential circuit with two D flip-flops, A and $B$; two inputs $x$ and $y$, and one output $z$, is described by the following input and output equations:

$$
\begin{aligned}
& -\mathrm{A}(\mathrm{t}+1)=\mathrm{x}^{\prime} \mathrm{y}+\mathrm{xA} \\
& -\mathrm{B}(\mathrm{t}+1)=\mathrm{x}^{\prime} \mathrm{B}+\mathrm{xA} \\
& -\mathrm{z}=\mathrm{B}
\end{aligned}
$$

a. Is the design in Mealy or Moore model?
b. Draw the diagram for the circuit.
c. Derive the state table.
d. Derive the state diagram.

## Task 1: Ans. a, b

- Moore model - output (z) depends only on state (B)
- Note $\mathrm{DA}=\mathrm{A}(\mathrm{t}+1)$ and $\mathrm{DB}=\mathrm{B}(\mathrm{t}+1)$



## Task 1: Ans. c

|  | Present State |  | Inputs |  | Next State |  |  | Output Z |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | B | X | Y |  |  | $B(t+1)$ |  |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |
|  | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  |
|  | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  |
|  | 0 | 1 | 0 | 0 | 0 | 1 | 1 |  |
|  | 0 | 1 | 0 | 1 | 1 | 1 | 1 |  |
|  | 0 | 1 | 1 | 0 | 0 | 0 | 1 |  |
|  | 0 | 1 | 1 | 1 | 0 | 0 | 1 |  |
|  | 1 | 0 | 0 | 0 | 0 | 0 | 0 |  |
|  | 1 | 0 | 0 | 1 | 1 | 0 | 0 |  |
|  | 1 | 0 | 1 | 0 | 1 | 1 | 0 |  |
|  | 1 | 0 | 1 | 1 | 1 | 1 | 0 |  |
|  | 1 | 1 | 0 | 0 | 0 | 1 | 1 |  |
|  | 1 | 1 | 0 | 1 | 1 | 1 | 1 |  |
|  | 1 | 1 | 1 | 0 | 1 | 1 | 1 |  |
|  | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
| owh@ieee.org |  |  |  |  |  |  |  |  |

## Task 1: Ans. d

- Two state variables (A, B) hence $22=4$ states.



## Task 2

- For the state table shown in next slide:
a. Can the circuit be designed with Moore model? Why?
b. Extend the table for design using JK flip-flops.
c. Derive the flip-flop input equations and output equation.
d. Draw the circuit diagram for the above design.


## Task 2 (State Table)



## Task 2: Ans. a, b

- No. The output (z) depends on both state and inputs, e.g. in state oo, the output can either be o (when inputs are 0o or 01) or 1 (when inputs are 10 or 11).
- In each row, look at changes in A \& B from present to next state. Determine the required values for JA, KA, JB and KB to give the change, by referring to excitation table of JK flip-flop.


## Task 2: Ans. b

| Present State | Inputs | Next State | Output |  | Inputs |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A B | X Y | DA DB | Z | JA | KA JB | KB |  |  |  |
| 00 | 00 | 00 | 0 | 0 | $\times 0$ | x |  |  |  |
| 00 | 01 | 01 | 0 | 0 | $\times 1$ | x |  |  |  |
| 0 | 10 | 10 | 1 | 1 | x 0 | x |  |  |  |
| 0 | 11 | 11 | 1 | 1 | x 1 | x |  |  |  |
| 01 | 00 | 01 | 1 | 0 | $x$ x | 0 |  |  |  |
| 01 | 01 | 10 | 1 | 1 | $x$ x | 1 |  |  |  |
| 01 | 10 | 10 | 0 | 1 | $x$ x | 1 | Exxitation Table |  |  |
| 01 | 11 | 0 | 0 | 0 | $x$ x | 1 |  |  |  |
| 10 | 00 | 11 | 1 | x | 01 | x | ${ }^{\text {Q(t) }}$ | ${ }^{\text {Q ( }+1)}$ ) | JK Operatio |
| 10 | 01 | 11 | 0 | $x$ | 01 | x | $\bigcirc$ | 0 |  |
| 10 | 10 | 11 | 1 | x | 01 | x | $\bigcirc$ | 。 |  |
| 10 | 11 | 10 | 0 | x | 00 | x | 1 | $1 \times$ | x 0 No Change |
| 11 | 00 | 0 | 0 | $x$ | 1 x | 1 |  |  |  |
| 1 | 01 | 0 | 1 | x | 1 x | 1 |  |  |  |
| 1 | 10 | 0 | 0 | x | 1 x | 1 |  |  |  |
| 1 | 11 | 01 | 1 | x | 1 x | 0 |  |  |  |
| owh@ieee.org |  |  | CO 2206 |  |  |  |  |  | 9 |

## Task 2: Ans. c

- Five equations to determine: Z, JA, KA, JB, KB. Input variables are $\mathrm{A}, \mathrm{B}, \mathrm{X}$ and Y .


Alternative: $\mathrm{J}_{\mathrm{A}}=\mathrm{XY} \mathrm{Y}^{\prime}+\mathrm{B}^{\prime} \mathrm{X}+\mathrm{BX}^{\prime} \mathrm{Y}$


A

$$
Z=A^{\prime} B^{\prime} X+A^{\prime} B X^{\prime}+A B Y+A B^{\prime} Y^{\prime}
$$



## Task 2: Ans. d

- DIY. Take note of the common clock connection. The circuit will have two J/K flip-flops.


## Task 3 \& 4

- Task 3: Design a sequential circuit with two D flip-flops A and B and one input X . When $\mathrm{X}=1$, the state of the circuit remains the same. When $\mathrm{X}=\mathrm{o}$, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00, and then repeats.
- Task 4: Use 4-bit binary counter with synchronous parallel load (in block diagram) and logic gates to design the following counters:
a. Modulo- 3 that counts $0,1,2$ repeatedly
b. Modulo-6 that counts $2,3,4,5,6,7$ repeatedly


## Task 3: Ans. 1

- Steps involved:
- Draw the state diagram based on requirements in the question
- Draw the state table from the state diagram - define the necessary columns: A, B, X, DA, DB
- Derive flip-flop input functions (DA, DB)
- Draw the circuit diagram


## Task 3: Ans. 2

- State diagram:



## Task 3: Ans. 3

- State table:

| Present State |  | Inputs | Next State |  |
| :--- | :--- | :--- | :--- | :---: |
| A | B | X | DA DB |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 1 | 0 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 |  | 1 | 0 |  |
| 1 |  |  |  |  |

## Task 3: Ans. 4

- Flip-flop input equations:

- Circuit diagram: DIY. Take note of the common clock connection. There shall be 2 D flip-flops.

