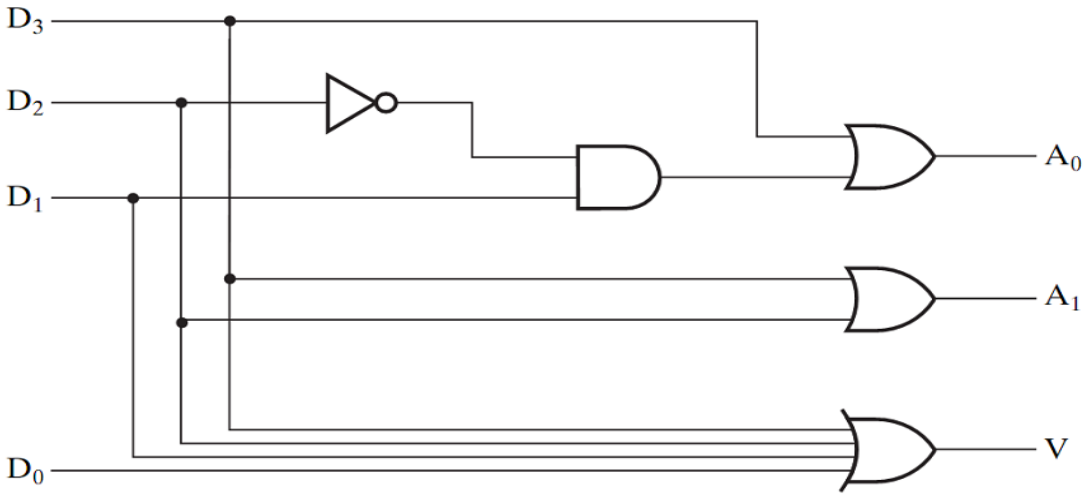
Tutorial 5 (lab based)
VHDL

CO 2206 Computer Organization

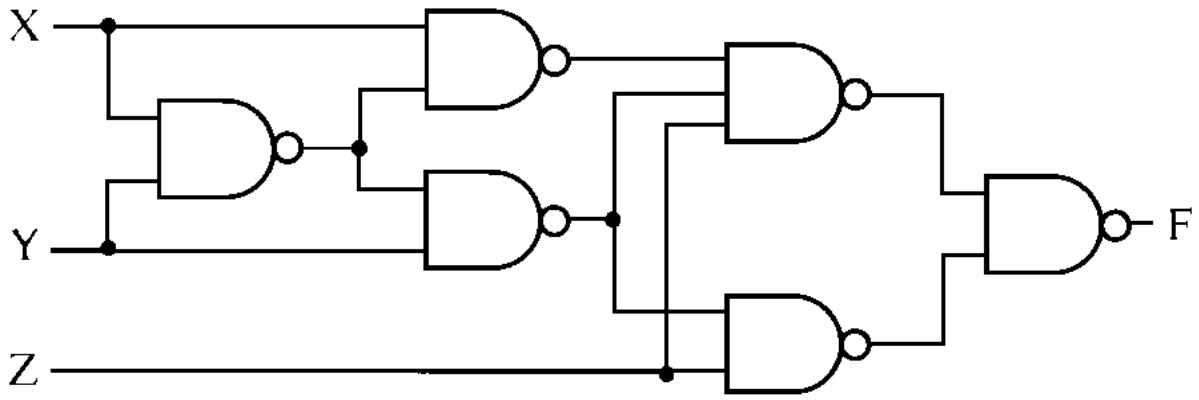
Task 1

- For the logic circuit given below,
  - Determine the Boolean function for A0, A1 and V.
  - Write a high-level behavioral VHDL description to describe it.
  - Write a structural VHDL description to describe it.



Task 2

- Write a dataflow description for the circuit in the figure below by using the Boolean equation for the output F.
- Write a test bench to simulate the operation of the circuit for all input combinations.



Task 3

- Find a logic diagram representing minimum two-level logic to implement the VHDL dataflow description below. Note that complemented inputs are available.

```
library ieee;
use ieee.std_logic_1164.all;
entity comb_ckt_2 is
    port (a, b, c, d, a_n, b_n, c_n, d_n: in std_logic;
        f, g: out std_logic);
-- a_n, b_n, ... are complements of a, b, ..., respectively
end comb_ckt_2;

architecture dataflow_1 of comb_ckt_2 is
begin
    f <= b and (a or (a_n and c)) or (b_n and c and d_n);
    g <= b and (c or (a_n and c_n) or (c_n and d_n));
end dataflow_1;
```

Task 4

- Write a high-level behavioral VHDL description for a 1-bit full adder.
- Write a structural VHDL description for a 1-bit adder-subtractor. Make you of the 1-bit full adder above as a component.
- Write a high-level behavioral VHDL description for a 1-bit adder-subtractor.