Tutorial 4 – Sample Solutions
Combinational Logic

CO 2206 Computer Organization

CLN Functional Block ICs

- **Task 1:** Determine (research for) the part numbers and descriptions for decoder, encoder, multiplexer, demultiplexer and full adder IC (TTL)
  - there will be different versions for each type of IC, e.g. different sizes of decoder
  - state up to three part number for each type (if available), which you feel will be useful (or make sense to you from what you learnt in the lectures)

Task 1. Ans (1)

- decoder -
  - 74138: 3 to 8-line Decoder/Demultiplexer
  - 74139: Dual 2 to 4-line Decoder
  - 74154: 4-Line to 16-Line Decoder/Demultiplexer
- encoder -
  - 74348: 8 to 3-line Priority Encoder with three-state outputs
  - 74748: 8 to 3-line priority encoder
  - 74148: 8-Line to 3-Line Priority Encoder

Task 1. Ans (2)

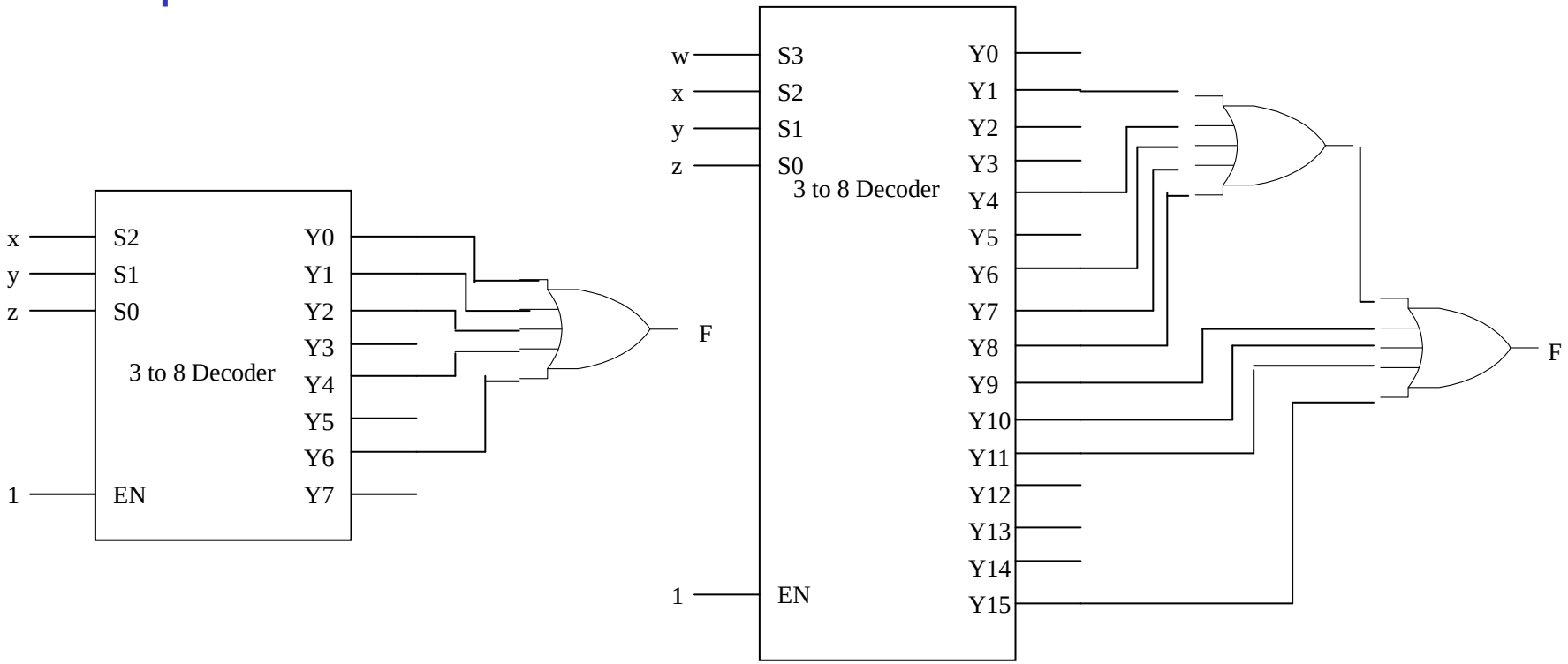
- multiplexer -
  - 74251: 8-line to 1-line Data Selector/Multiplexer with complementary three-state outputs
  - 74253: Dual 4-line to 1-line Data Selector/Multiplexer with three-state outputs
  - 74356: 8 to 1-line Data Selector/Multiplexer with Edge-Triggered Register, three-state outputs
- demultiplexer -
  - same as decoder
- full adder IC -
  - 74183: Dual Carry-Save Full Adder
  - 74283: 4-bit Binary Full adder
  - 74385: Quad 4-bit Adder/Subtractor

Using the Functional Blocks

- **Task 2:** Implement the following functions using an appropriate decoder:
  - $F(x,y,z) = \sum m(0,1,2,4,6)$
  - $F(w,x,y,z) = \Sigma m(1,4,6,7,8,9,10,11,15)$
- **Task 3:** Implement the above functions using an appropriate Multiplexer.
- **Task 4:** Design a circuit that multiplies a 4-bit multiplicand by the constant 1010

Task 2. Ans

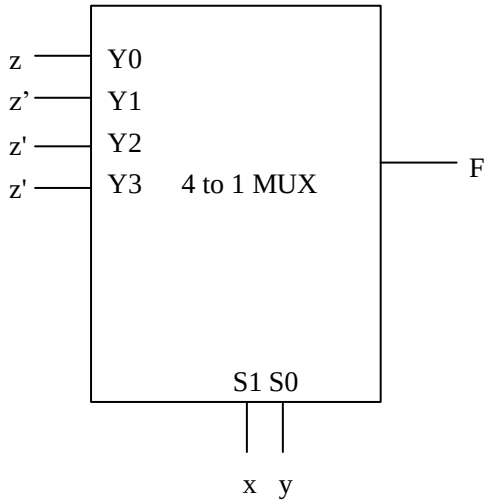
- F(x,y,z) has 3 input variables hence requiring a 3-to-8 decoder; F(w,x,y,z) has 4 input variables hence requiring a 4-to-16 decoder



Task 3. Ans (1)

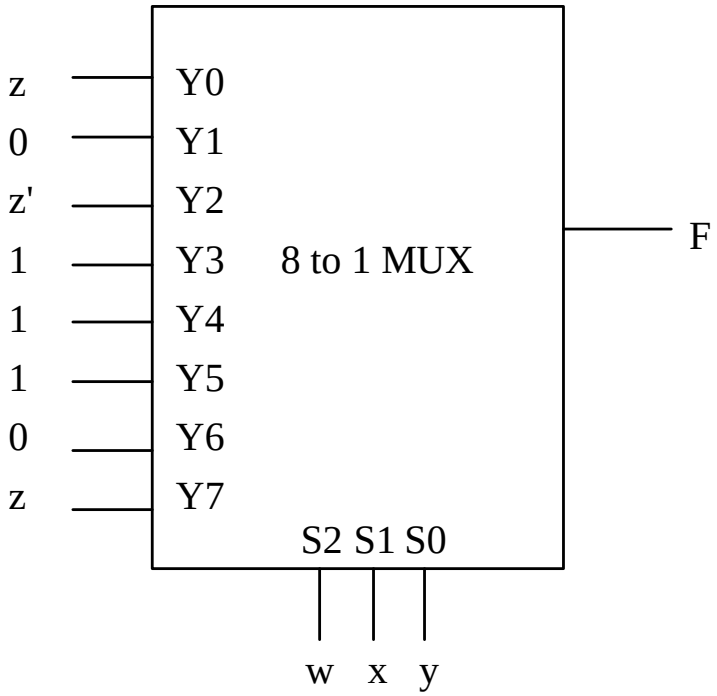
- One input variable is used to form the functions for the inputs of the MUX and the remaining inputs (i.e. 2) are used to select these functions accordingly; hence we require a 2^2 or 4-1 MUX.

x	y	z	F	
0	0	0	0	F = z
0	0	1	1	
0	1	0	1	F = z’
0	1	1	0	
1	0	0	1	F = z’
1	0	1	0	
1	1	0	1	F = z’
1	1	1	0	



Task 3. Ans (2)

w	x	y	z	F	
0	0	0	0	0	F = z
0	0	0	1	1	
0	0	1	0	0	F = 0
0	0	1	1	0	
0	1	0	0	1	F = z’
0	1	0	1	0	
0	1	1	0	1	F = 1
0	1	1	1	1	
1	0	0	0	1	F = 1
1	0	0	1	1	
1	0	1	0	1	F = 1
1	0	1	1	1	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	0	F = z
1	1	1	1	1	



Task 4. Ans.1

- Generally

				B_3	B_2	B_1	B_0
				A_3	A_2	A_1	A_0
				A_0B_3	A_0B_2	A_0B_1	A_0B_0
			A_1B_3	A_1B_2	A_1B_1	A_1B_0	
		A_2B_3	A_2B_2	A_2B_1	A_2B_0		
	A_3B_3	A_3B_2	A_3B_1	A_3B_0			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Task 4. Ans.2

- Figure shows the general circuit. It can be easily modified for different number of bits for addend or augend. The required answer for this question shall be the circuit above modified with input B3B2B1B0 replaced by the constant Augend of “1010”.